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Tutorial title: Large and Very Large Scale Intractable Combinatorial VLSI Physical Design Problems: How to solve them with high quality?

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Abstract of the tutorial: Rapid growth of electronic circuit complexity requires a further search for new effective approaches to solve CAD problems. The methods for combinatorial optimization are especially important for VLSI, SoC and NoC physical design. In this case, partitioning, packaging, placement and routing are very important problems. Identical input data is the common peculiarity of these problems. The idea was to operate not by original elements, the number of which is extraordinarily high, but by clusters that could be mathematically described by macromodels. This enables us, first of all, to essentially decrease the size of the problem, facilitating a solution and reducing the calculation consumption, and, secondly, to considerably improve the quality of the solution, to more easy provide trapping into the zone of the global optimum.

New basic algorithms were developed for

- hierarchical circuit clustering and decomposition;
- partitioning: initial (serial, parallel-serial and dichotomy) and its optimization;
- packaging (serial and parallel-serial);
- placement (hierarchical decomposition and scanning area methods).

The proposed algorithms have some new properties, for example, they can be effective in choosing the most appropriate number of partitions into which it is necessary to divide the circuit; arbitrary division coefficient (ratio) can be chosen for partitioning; the same procedures can be used for initial solution and their optimization. The suggested algorithms have near linear computational complexity and provide good quality of solutions. For all test cases investigated, the results are not worse, and in many cases they are better then those obtained by other known methods. For some cases, the optimal results were obtained for the first time.

Expected background for the audience: academicians, university faculties, researchers, and graduate students

Brief bio-data of the presenter: Roman P. Bazylevych received the the Doctor of Engineering Sciences degree in computer science from the Leningrad Electrotechnical Institute in 1984. In 1967 he joined the Lviv Polytechnic State University where he is currently the Full Professor of Software Department. His research interests include Physical Design Automation of microelectronic circuits (partitioning, placement and routing problems), combinatorial optimization of intractable problems. He authored the book "Decomposition and Topological Methods for Physical Design Automation of Electronic Devices". He is a full member of the Shewchenko Scientific Society, Academician of the Academy of Engineering Sciences of Ukraine, Fellow member of the

IEE, member of the ACM. Dr.R.Bazylevych conducted research at the Harvard University (2000-2001) and the University of California at San-Diego (1995-1996). Authored 3 scientific monographs, 2 textbooks, has 350 scientific publications, 11 patents, supervisor of 11 Ph.D. and one D.Sc. dissertation, scientific Leader of 45 research projects (Grants and Contracts).